What is Claimed is:

1. An integrated memory, comprising:

a memory cell array, the memory cell array including a plurality of word lines for the selection of memory cells and a plurality of bit lines for reading out or writing data signals of the memory cells, the bit lines being organized in bit line pairs, the bit lines of a bit line pair crossing one another at a crossing location, the bit lines running parallel to one another;

a sense amplifier, the sense amplifier being connected to one of the bit line pairs at one end of the bit line pair; and

at least one activatable isolation circuit, the isolation circuit being switched into one of the bit line pairs, wherein the activated state during an access to the memory cell array, the isolation circuit isolating a part of one of the bit line pairs which is more remote from the sense amplifier, from the sense amplifier circuit being arranged at a first distance from the crossing location and at a second distance from the sense amplifier, the first distance being less than the second distance.

2. The integrated memory as claimed in claim 1, wherein the at least one isolation circuit is arranged within a region, the region being significantly smaller relative to the memory cell array, the region being arranged centrally relative to the longitudinal extent of the relevant bit line pair.

3. The integrated memory as claimed in claim 1 wherein the at least one isolation circuit is activated by a word line decoder for the selection of one of the word lines for the memory access.

4. The integrated memory as claimed in claim 1, wherein

at least one first and second sense amplifier strip are provided within the memory cell array,

the bit line pairs, are alternately connected to a sense amplifier of the first sense amplifier strip and a sense amplifier of the second amplifier strip in the longitudinal direction of the sense amplifier strips, and

a plurality of isolation circuits are provided, the isolation circuits being arranged and designed such that, in the activated state, in the longitudinal direction of the sense amplifier strips, for each second bit line pair, a part of the respective bit line pair, which is more remote from the respective sense amplifier, can be isolated from the sense amplifier by one of the isolation circuits.